METHOD AND STRUCTURE TO USE AN ETCH RESISTANT LINER ON TRANSISTOR GATE STRUCTURE TO ACHIEVE HIGH DEVICE PERFORMANCE

ABSTRACT

An etch resistant liner covering sidewalls of a transistor gate stack and along a portion of the substrate at a base of the transistor gate stack. The liner prevents silicide formation on the sidewalls of the gate stack, which may produce electrical shorting, and determines the location of silicide formation within source and drain regions within the substrate at the base of the transistor gate stack. The liner also covers a resistor gate stack preventing silicide formation within or adjacent to the resistor gate stack.